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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,728	SYMES, DOMINIC HUGO	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- Th MAILING DATE of this communication appears on the cover sh t with th correspond nc addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment and Change of Address as received on 11/24/2004.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The examiner recommends incorporating into the title the operation described in claim 1.

Drawings

4. The drawings are objected to because of the following minor informalities: In Fig.4, the arrows at the top right (directly underneath the letter "k") should be pointing left, thereby signifying a left shift, as opposed to a right shift.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes

made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 14 is objected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More specifically, the preamble of claim 14 should be reworded because it is not clear what the meaning is behind "given by" and how it relates to the three steps performed.

7. Claim 15 is objected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. More specifically, the preamble of claim 15 should be reworded because it is not clear what the meaning is behind "given by" and how it relates to the three steps performed.

8. Claim 14 recites the limitation "said data word Rn" in line 3. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 14 recites the limitation "said data word Rm" in line 5. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 15 is objected to because of the following informalities: In line 2, replace "said a computer program" with --said computer program--. Appropriate correction is required.

11. Claim 15 recites the limitation "the steps" in line 3. There is insufficient antecedent basis for this limitation in the claim.

12. Claim 15 recites the limitation "said data word Rn". There is insufficient antecedent basis for this limitation in the claim.

13. Claim 15 recites the limitation "said data word Rm". There is insufficient antecedent basis for this limitation in the claim.

Maintained Rejections

14. Applicant has failed to overcome the prior art rejections set forth in the previous Office Action. Consequently, these rejections are respectfully maintained by the examiner and are copied below for applicant's convenience. Also, a new rejection is made for claim 15 to reflect the amendments made by applicant.

Claim Rejections - 35 USC § 112

15. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

16. Claim 15 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. More specifically, the examiner has been unable to find in applicant's specification, the disclosure of a type of computer-readable medium on which a computer program of claim 15 may be stored.

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

18. Claims 1-12 and 14-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Intel, "IA-64 Application Developer's Architecture Guide," May 1999 (herein referred to as Intel).

19. Referring to claim 1, Intel has taught apparatus for processing data, said apparatus comprising:

(i) a shifting circuit. See page 7-158 and note that data is shifted.

(ii) a bit portion selecting and combining circuit. Again from page 7-158, note that portions are selected and combined.

(iii) an instruction decoder responsive to an instruction to control said shifting circuit and said bit portion selecting and combining circuit for performing an operation upon a data word Rn and a

data word Rm (it is inherent that an instruction decoder exists in order to decode instructions prior to execution. The decoder, in response to the pshradd2 instruction, shown in page 7-158, will control the system such that the disclosed operation will be performed), wherein said operation yields a value given by:

(a) selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn. See page 7-158 and note that the most significant bits of register R3 (Rn) are selected and stored in array "y", thereby forming a first portion, which depending on interpretation, comprises either 16 or 32 bits. These bits, since they are the most significant, start from one end of Rn.

(b) selecting a second portion of bit length B of said data word Rm subject to an arithmetic right shift specified as a shift operand within said instruction. See page 7-158 and note that the least significant bits of register R2 (Rm) are selected and stored in array "x", thereby forming a first portion, which depending on interpretation, comprises either 16 or 32 bits. This portion is then subject to a right shift by count2 bits, which is an operand specified within the instruction. This shift is an arithmetic shift because sign bits are shifted in (in a logical shift, only 0s are shifted in).

(c) combining said first portion and said second portion to form respective different bit position portions of an output data word Rd. From page 7-158, it can be seen that the two portions are modified via addition and then concatenated (combined) and stored in destination R1 (Rd). It should be noted that the use of the word "comprising" in applicant's claim allows for anticipation by Intel even though Intel's portions are modified before they are combined.

20. Referring to claim 2, Intel has taught an apparatus as described in claim 1. Intel has further taught that said first portion extends from a most significant bit end of said data word Rn. For instance, see page 7-158 and note that the 32 most significant bits of register R3 (Rn) are selected and stored in y[3] and y[2], each holding 16 of the 32 bits. These bits, since they are the most significant, start from one end of Rn.

21. Referring to claim 3, Intel has taught an apparatus as described in claim 1. Intel has further taught that said first portion extends from a least significant bit end of said data word Rn. Even though the example given in the rejection of claim 1 above includes selecting the most significant bits of Rn, the least significant bits of Rn are also selected and stored in array "y". These least significant bits may alternatively be referred to as the first portion.

22. Referring to claim 4, Intel has taught an apparatus as described in claim 1. Intel has further taught that said shift operand can specify a number of bit-positions representing an amount of arithmetic right shift to apply to said data word Rm. See page 7-158 and note that the count2 operand specifies any of 1, 2, or 3 for the amount of bits the data will be shifted.

23. Referring to claim 5, Intel has taught an apparatus as described in claim 1. Intel has further taught that said first portion and said second portion abut within said output data word Rd. See page 7-158 and note at the bottom of code snippet that the portions, after being modified, are concatenated and stored in the 64-bit register R1 (Rd).

24. Referring to claim 6, Intel has taught an apparatus as described in claim 5. Intel has further taught that said output data word has a bit length of C and C = A+B. Note from page 7-158 that the output data word is 64 bits in length (four additions occur on four 16-bit words) and the first portion A and second portion B are each 32 bits in length.

25. Referring to claim 7, Intel has taught an apparatus as described in claim 6. Intel has further taught that A = B. Both A and B are 32-bit portions.

26. Referring to claim 8, Intel has taught an apparatus as described in claim 1. Intel has further taught that A = 16. See page 7-158 and note that the first portion selected from R3 (Rn) comprises 16 bits. More specifically, the first portion would be bits 63:48 of R3, for instance, which are then stored in y[3].

27. Referring to claim 9, Intel has taught an apparatus as described in claim 1. Intel has further taught that B = 16. See page 7-158 and note that the second portion selected from R2 (Rm) comprises 16 bits. More specifically, the second portion would be bits 15:0 of R2, for instance, which are then stored in x[0].

28. Referring to claim 10, Intel has taught an apparatus as described in claim 1. Intel has further taught that said instruction is a single-instruction-multiple-data instruction. See page 7-158 and note that with one instruction, multiple additions are formed.

29. Referring to claim 11, Intel has taught an apparatus as described in claim 1. Intel has further taught that said instruction combines a data value pack operation with a shift operation. See page 7-158 and note that data is at least shifted and packed into a destination operand R1 (Rd).

30. Referring to claim 12, Intel has taught an apparatus as described in claim 1. Intel has further taught that said shifting circuit is upstream of said selecting and combining circuit in a data path of said apparatus. Looking at page 7-128, it can be seen (in the operation program) that the shifting occurs before the combination. That is, the shifting is in the for loop while the

combination is outside and after the for loop. Therefore, the shifting circuit is upstream of the selecting and combining circuit.

31. Referring to claim 14, Intel has taught a method of data processing, said method comprising the steps of decoding and executing an instruction that yields a value given by:

(i) selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn. See page 7-158 and note that the most significant bits of register R3 (Rn) are selected and stored in array "y", thereby forming a first portion, which depending on interpretation, comprises either 16 or 32 bits. These bits, since they are the most significant, start from one end of Rn.

(ii) selecting a second portion of bit length B of said data word Rm subject to an arithmetic right shift specified as a shift operand within said instruction. See page 7-158 and note that the least significant bits of register R2 (Rm) are selected and stored in array "x", thereby forming a first portion, which depending on interpretation, comprises either 16 or 32 bits. This portion is then subject to a right shift by count2 bits, which is an operand specified within the instruction. This shift is an arithmetic shift because sign bits are shifted in (in a logical shift, only 0s are shifted in).

(iii) combining said first portion and said second portion to form respective different bit position portions of an output data word Rd. From page 7-158, it can be seen that the two portions are modified via addition and then concatenated (combined) and stored in destination R1 (Rd). It should be noted that the use of the word "comprising" in applicant's claim allows for anticipation by Intel even though Intel's portions are modified before they are combined.

32. Referring to claim 15, Intel has taught a computer program provided on a computer-readable medium, said computer program for controlling a computer to perform the steps of decoding and executing an instruction that yields a value given by:

(i) selecting a first portion of bit length A of said data word Rn extending from one end of said data word Rn. See page 7-158 and note that the most significant bits of register R3 (Rn) are selected and stored in array "y", thereby forming a first portion, which depending on interpretation, comprises either 16 or 32 bits. These bits, since they are the most significant, start from one end of Rn.

(ii) selecting a second portion of bit length B of said data word Rm subject to an arithmetic right shift specified as a shift operand within said instruction. See page 7-158 and note that the least significant bits of register R2 (Rm) are selected and stored in array "x", thereby forming a first portion, which depending on interpretation, comprises either 16 or 32 bits. This portion is then subject to a right shift by count2 bits, which is an operand specified within the instruction. This shift is an arithmetic shift because sign bits are shifted in (in a logical shift, only 0s are shifted in).

(iii) combining said first portion and said second portion to form respective different bit position portions of an output data word Rd. From page 7-158, it can be seen that the two portions are modified via addition and then concatenated (combined) and stored in destination R1 (Rd). It should be noted that the use of the word "comprising" in applicant's claim allows for anticipation by Intel even though Intel's portions are modified before they are combined.

It should be noted that the instruction shown on page 7-158 of Intel would inherently be found in a computer program on a computer-readable medium.

Claim Rejections - 35 USC § 103

33. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Intel, as applied above.

35. Referring to claim 13, Intel has taught an apparatus as described in claim 12. Intel has not explicitly taught that said selecting and combining circuit is disposed in parallel to an arithmetic circuit within said data path. However, from a software point of view, Official Notice is taken that pipelining and its advantages are well known and accepted in the art. More specifically, in a pipelined machine, multiple instructions execute in parallel using different components within the system. This increases throughput because at any given time, multiple instructions are executing, whereas with serial execution, only one instruction is executed at a time. Therefore, in order to increase throughput, it would have been obvious to one of ordinary skill in the art at the time of the invention to dispose the selecting and combining circuit in parallel to an arithmetic circuit within said data path. By doing so, one instruction utilizes the arithmetic unit while another instruction utilizes the shifter. If these resources are able to operate on data in parallel, then the resources are disposed in parallel. Clearly, resources are more efficiently utilized as they are not sitting idle as often as they would be during serial execution.

On the other hand, if taken from a hardware point of view, the examiner asserts that it is

merely a design choice as to how each component on the chip should be arranged. As shown in In re Japikse 86 USPQ 70 (CCPA 1950), to shift location of parts is generally not given patentable weight or would have been an obvious improvement (perhaps to minimize total chip area consumed and/or wire length). Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to place the arithmetic circuit in parallel with the selecting and combining circuit.

Response to Arguments

36. Applicant's arguments filed on November 24, 2004, have been fully considered but they are not persuasive.

37. Applicant argues the novelty/rejection of claim 1 on pages 16-17 of the remarks, in substance that:

> "Applicant notes that at least the copy of Intel provided by the Patent Office included only pages 7-117, 135, 150, 158, 169 and 182-184. As a result of the partial copy, it is entirely possible that there are other and more apparent reasons why Intel is not a reference against these claims under the provisions of 35 USC #102."
>
> "However, even in view of the partial copy of the Intel document, it is apparently not an anticipatory reference. For example, the Examiner at page 7 of the Official Action admits that 'Intel's portions are modified before they are combined.' The Examiner suggests that he uses the word 'comprising' in Applicant's claim as a rationale for otherwise ignoring the teaching of the Intel reference. The Examiner's rationale is seriously flawed for the following reasons: Applicant's independent claim 1 specifies three elements, i.e., (i) a shifting circuit; (ii) a bit portion selecting and combining circuit; and (iii) an instruction decoder. As a limitation on the instruction decoder, it performs an operation upon the data words Rn and Rm to yield a value given by the recited three-step process. It is noted that the phrase "said apparatus comprising" refers to the three structures recited in the claim. The three method steps serve to define the value provided by the instruction decoder. As will be readily apparent, any modification of the portions recited in the method for determining the value will change the value which is otherwise specified in claim 1. The Examiner admits that in the Intel teaching the values 'are modified before they are combined.' As a result, they cannot possibly be combined so as to provide the value recited in Applicant's claim."

38. These arguments are not found persuasive for the following reasons:

a) Regarding the first argument, the Intel reference is nearly 500 pages long. Consequently, only the pertinent portions were supplied to applicant while the rest were deemed irrelevant at this point by the examiner.

b) Regarding the second argument, the examiner would like to direct applicant's attention to section 2111.03 of the MPEP, which states:

"The transitional phrases "comprising", "consisting essentially of" and "consisting of" define the scope of a claim with respect to what unrecited additional components or steps, if any, are excluded from the scope of the claim.

The transitional term "comprising", which is synonymous with "including," "containing," or "characterized by," is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. See, e.g., > Invitrogen Corp. v. Biocrest Mfg., L.P., 327 F.3d 1364, 1368, 66 USPQ2d 1631, 1634 (Fed. Cir. 2003) ("The transition comprising' in a method claim indicates that the claim is open-ended and allows for additional steps.");< Genentech, Inc. v. Chiron Corp., 112 F.3d 495, 501, 42 USPQ2d 1608, 1613 (Fed. Cir. 1997) ("Comprising" is a term of art used in claim language which means that the named elements are essential, but other elements may be added and still form a construct within the scope of the claim.); Moleculon Research Corp. v. CBS, Inc., 793 F.2d 1261, 229 USPQ 805 (Fed. Cir. 1986); In re Baxter, 656 F.2d 679, 686, 210 USPQ 795, 803 (CCPA 1981); Ex parte Davis, 80 USPQ 448, 450 (Bd. App. 1948) **("comprising" leaves "the claim open for the inclusion of unspecified ingredients even in major amounts")**."

It should be noted (from the above passage, and most specifically, the bolded portion) that "comprising" affects the whole claim. If applicant does not want the values to be modified before their combination, then such specifics should be claimed. However, if this is the case, applicant should be careful, because by right shifting the second portion before combination, applicant is, in effect, doing modification before combination.

Conclusion

39. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH

David J. Huisman
December 13, 2004

RICHARD L. ELLIS
PRIMARY EXAMINER